MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)

II B.Tech I Semester (MR20-2020-21 Batch) Mid Term Examinations-II, February-2022

Subject Code & Name: - A0508 & **Computer Organization and Architecture** Max. Marks: **25M**

Branch: Common to **CSE,CS,DS,IOT,AIML,IT** Time: **90 Mins** Date:

Answer ALL the Questions

S NO.	Questions	Marks	BT Level	CO
	Module-3			
1	Use different instruction format and evaluate the expression Y=(A-B)/(C+D*E)	5	3	3
2	Explain about Addressing Modes with an Numerical Example?	5	2	3
3	Distinguish between data transfer and data manipulation instructions.	5	2	3
4	Classify the different program control instructions	5	2	3
S NO.	**Questions**	**Marks**	**BT Level**	**CO**
	Module-4			
1	Classify the complements that are used in digital computers.	5	2	4
2	Describe the two different types of data that computer uses	5	2	4
3	Explain the fixed point representation and floating point representation	5	2	4
4	Design the flow chart for addition and subtraction operations with example.	5	6	4
5	Evaluate multiplication of two numbers using Multiplication algorithm with a numerical example.	5	5	4
6	Design the flow chart for Booths Multiplication algorithm with an example	5	6	4
7	Use the flow chart for division algorithm and solve AQ=0111000000 divided by B=10001	5	3	4
8	Explain decimal arithmetic operations.	5	2	4
S NO.	**Questions**	**Marks**	**BT Level**	**CO**
	Module-5			
1	Analyze the 3 different mapping processes used in cache memory organization.	5	4	5
2	Explain Daisy Chaining and Parallel Priority Interrupt with the help of a neat sketch	5	2	5
3	Interpret the Memory Connection to CPU by using Memory Address Mapping of RAM Chip and ROM Chip	5	3	5
4	Explain a) Auxiliary Memory b) Associate Memory	5	2	5
5	Sketch the block diagram of DMA using DMA Controller	5	3	5
6	Explain the different types of modes of transfer in detail	5	2	5
7	Describe the asynchronous data transfer	5	2	5
8	Explain memory hierarchy in memory organization	5	2	5

Prepared By Name:

Signature: **HOD Signature**

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S. NO.	Questions	Ans
	Model-3	
1	The fastest data access is provided using _____. a) Caches b) DRAM's c) SRAM's d) Registers	[ ]
2	The effectiveness of the cache memory is based on the property of a)Locality of reference b) Memory localization c) Memory size d) None of the above	[ ]
3	The correspondence between the main memory blocks and those in the cache is given by a) Hash function b) Locale function c) Mapping function d) Assign function	[ ]
4	The algorithm to remove and place new contents into the cache is called a) Replacement algorithm b) Updation c) Renewal algorithm d) None of the above	[ ]
5	The bit used to signify that the cache location is updated is _____. a) Dirty bit b) Update bit c) Reference bit d) Flag bit	[ ]
6	The last on the hierarchy scale of memory devices is _____. a) Main memory b) Secondary memory c) TLB d) Flash drives	[ ]
7	In memory interleaving, the lower order bits of the address is used to a) Get the data b) Get the address of the data within the module c) Get the address of the module d) None of the above	[ ]
8	The number of successful accesses to memory stated as a fraction is called as a) Hit rate b) Miss rate c) Success rate d) Access rate	[ ]
9	The number of failed attempts to access memory, stated in the form of fraction is called as a) Hit rate b) Miss rate c) Failure rate d) Delay rate	[ ]
10	In associative mapping during LRU, the counter of the new block is set to '0' and all the others are incremented by one, when _____ occurs. a) Delay rate b) Miss rate c) Hit rate d) Delayed rate	[ ]
11	The extra time needed to bring the data into memory in case of a miss is called as a) Delay rate b) Miss rate c) Hit rate d) Delayed rate	[ ]
12	The key factor/s in commercial success of a computer is/are _____. a) Performance b) Cost c) Speed d) Both a and b	[ ]
13	The main objective of the computer system is a) To provide optimal power operation b) To provide best performance at low cost c) To provide speedy operation at low power consumption d) All the above	[ ]
14	The main purpose of having memory hierarchy is to a) Reduce access time b) Reduce propagation time c) Provide large capacity d) Both a and b	[ ]
15	The program is divided into operable parts called as _____. a) Frames b) Segments c) Pages d) Sheets	[ ]
16	The techniques which move the program blocks to or from the physical memory is called as a) Paging b) Virtual memory organization c) Overlays d) Framing	[ ]
17	The binary address issued to data or instructions are called as _____. a) Physical address b) Location c) Relocatable address d) Logical address	[ ]
18	_____is used to implement virtual memory organization. a) Page table b) Frame table c) MMU d) None of the above	[ ]
19	_____ translates logical address into physical address. a) MMU b) Translator c) Compiler d) Linker	[ ]
20	The main aim of virtual memory organization is a) To provide effective memory access b) To improve the execution of the program c) To provide better memory transfer d) All of the above	[ ]

21	The virtual memory basically stores the next segment of data to be executed on the a) Secondary storage b) Disks c) RAM d) ROM	[ ]
22	For the synchronization of the read head, we make use of a _____. a) Framing bit b) Synchronization bit c) Clock d) Dirty bit	[ ]
23	Floating-point numbers are normally a multiples of size of a) Bit b) Nibble c) Word d) Byte	[ ]
24	A 4 digit BCD number can be represented with the help of a) 10 bits b) 16 bits c) 8 bits d) 12 bits	[ ]
25	Any electronic holding place where data can be stored and retrieved later whenever required is a) Memory b) Drive c) Disk d) Circuit	[ ]
	Model-4	
26	The logic operations are implemented using _____ circuits. a) Bridge b) Logical c) Combinational d) Gate	[ ]
27	The carry generation function: ci + 1 = yici + xici + xiyi, is implemented in a) Half adders b) Full adders c) Ripple adders d) Fast adders	[ ]
28	The carry in the ripple adders, (which is true) a) Are generated at the beginning only b) Is generated at the end of each operation c) Must travel through the configuration d) None of the above	[ ]
29	In full adders the sum circuit is implemented using _____ gates. a) AND&OR b) NAND c) XOR d) XNOR	[ ]
30	The usual implementation of the carry circuit involves _____ gates. a) AND&OR b) XOR c) NAND d) XNOR	[ ]
31	A _____ gate is used to detect the occurrence of an overflow. a) NAND b) XOR c) XNOR d) AND	[ ]
32	In a normal adder circuit the delay obtained in generation of the output is a) 2n + 2 b) 2n c) n + 2 d) None of the above	[ ]
33	The final sum of the numbers, 0110 & 0110 is a) 1101 b) 1111 c) 1001 d) 1010	[ ]
34	The delay reduced to in the carry look ahead adder is _____. a) 5 b) 8 c) 10 d) 2n	[ ]
35	We make use of _____ circuits to implement multiplication. a) Flip flops b) Combinatorial c) Fast adders d) None of the above	[ ]
36	The multiplier is stored in _____. a) PC Register b) Shift register c) Cache d) None of the above	[ ]
37	The _____ is used to co-ordinate the operation of the multiplier. a) Controller b) Coordinator c) Control sequencer d) None of the above	[ ]
38	The multiplicand and the control signals are passed through to the n-bit adder via a) MUX b) DEMUX c) Encoder d) Decoder	[ ]
39	The method used to reduce the maximum number of summands by half is a) Fast multiplication b) Bit-pair recording c) Quick multiplication d) None	[ ]
40	CSA stands for a) Computer Speed Addition b) Computer Service Architecture c) Carry Save Addition d) None of the above	[ ]
41	The numbers written to the power of 10 in the representation of decimal numbers are called as a) Height factors b) Size factors c) Scale factors d) None of the above	[ ]
42	If the decimal point is placed to the right of the first significant digit, then the number is called as a) Orthogonal b) Normalized c) Determinate d) None of the above	[ ]
43	_____ constitute the representation of the floating number a) Sign b) Significant digits c) Scale factor d) All of the above	[ ]
44	The sign followed by the string of digits is called as _____. a) Significant b) Determinant c) Mantissa d) Exponent	[ ]
45	In IEEE 32-bit representations, the mantissa of the fraction is said to occupy _____ bits. a) 24 b) 23 c) 20 d) 16	[ ]
46	The 32 bit representation of the decimal number is called as ____.	[ ]

	a) Double-precision b) Single-precision c) Extended format d) None	
47	In 32 bit representation the scale factor is a range of _____. a) -128 to 127 b) -256 to 255 c) 0 to 255 d) None of the above	[ ]
48	When the processor executes multiple instructions at a time it is said to use ___ a) Single issue b) Multiplicity c) Visualization d) Multiple issue	[ ]
49	The _____ plays a very vital role in case of super scalar processors. a) Compilers b) Motherboard c) Memory d) Peripherals	[ ]
50	In super-scalar processors, _____ mode of execution is used. a) In-order b) Post order c) Out of order d) None of the mentioned	[ ]
51	In memory-mapped I/O… a) The I/O devices and the memory share the same address space b) The I/O devices have a separate address space c) The memory and I/O devices have an associated address space d) A part of the memory is specifically set aside for the I/O operation	[ ]
52	The usual BUS structure used to connect the I/O devices is a) Star BUS structure b) Single BUS structure c) Multiple BUS structure d) Node to Node BUS structure	[ ]
53	The advantage of I/O mapped devices to memory mapped is a) The former offers faster transfer of data b) The devices connected using I/O mapping have a bigger buffer space c) The devices have to deal with fewer address lines d) No advantage as such	[ ]
54	To overcome the lag in the operating speeds of the I/O device and the processor we use a) Buffer spaces b) Status flags c) Interrupt signals d) Exceptions	[ ]
55	The method of accessing the I/O devices by repeatedly checking the status flags is a) Program-controlled I/O b) I/O mapped c) Memory-mapped I/O d) None	[ ]
56	The method which offers higher speeds of I/O transfers is a) Interrupts b) Memory mapping c) Program-controlled I/O d) DMA	[ ]
57	The process where in the processor constantly checks the status flags is called as a) Polling b) Inspection c) Reviewing d) Echoing	[ ]
58	As the instructions can deal with variable size operands we use _____ to resolve this a) Delimiter b) Size indicator mnemonic c) Special assemblers d) None	[ ]
59	The starting address is denoted using _____ directive a) EQU b) ORIGIN c) ORG d) PLACE	[ ]
60	The constant can be declared using ____ directive a) DATAWORD b) PLACE c) CONS d) DC	[ ]
61	To allocate a block of memory we use ____ directive a) RESERVE b) DS c) DATAWORD d) PLACE	[ ]
62	The Branch instruction in 68000 provides how many types of offsets? a) 3 b) 1 c) 0 d) 2	[ ]
63	The DMA transfers are performed by a control circuit called as a) Device interface b) DMA controller c) Data controller d) Overlooker	[ ]
64	In DMA transfers, the required signals and addresses are given by the a) Processor b) Device drivers c) DMA controllers d) The program itself	[ ]
65	The DMA controller has _____ registers a) 4 b) 2 c) 3 d) 1	[ ]
66	The controller is connected to the ____ a) Processor BUS b) System BUS c) External BUS d) None of the above	[ ]
67	The technique where the controller is given complete access to main memory is a) Cycle stealing b) Memory stealing c) Memory Con d) Burst mode	[ ]
68	To overcome the conflict over the possession of the BUS we use _____ a) Optimizers b) BUS arbitrators c) Multiple BUS structure d) None	[ ]

69	The registers of the controller are _____ a) 64 bits b) 24 bits c) 32 bits d) 16 bits	[ ]
70	The DMA transfer is initiated by _____ a) Processor b) The process being executed c) I/O devices d) OS	[ ]
71	_____ interrupt method uses register whose bits are set separately by interrupt signal for each device a) Parallel priority interrupt b) Daisy chaining c) Serial priority interrupt d) None of the above	[ ]
72	____ register is used for the purpose of controlling the status of each interrupt request in parallel priority interrupt a) Mass b) Mark c) Make d) Mask	[ ]
73	Interrupts initiated by an instruction is called as a) Internal b) External c) Hardware d) Software	[ ]
74	The signals that are provided to maintain proper data flow and synchronization between the data transmitter and receiver are called as _____ signals. a) Handshaking b) Control c) Input d) None	[ ]
75	The example of output device is a) CRT display b) 7-segment display c) Printer d) All the above	[ ]
	Model-5	
76	_____ have been developed specifically for pipelined systems. a) Utility software b) Speed up utilities c) Optimizing compilers d) None	[ ]
77	The pipelining process is also called as _____. a) Superscalar operation b) Assembly line operation c) Von Neumann cycle d) None	[ ]
78	The fetch and execution cycles are interleaved with the help of _____. a) Modification in processor architecture b) Special unit c) Clock d) Control unit	[ ]
79	Each stage in pipelining should be completed within ____ cycle. a) 1 b) 2 c) 3 d) 4	[ ]
80	Size of the _____ memory mainly depends on the size of the address bus. a) Main b) Virtual c) Secondary d) Cache	[ ]
81	If a unit completes its task before the allotted time period, then a)It'll perform some other task in the remaining time b)Its time gets reallocated to different task c)It'll remain idle for the remaining time d)None of the mentioned	[ ]
82	To increase the speed of memory access in pipelining, we make use of a)Special memory locations b) Special purpose registers c) Cache d) Buffers	[ ]
83	The iconic feature of the RISC machine among the following is _____ a)Reduced number of addressing modes b) Increased memory size c)Having a branch delay slot d)All of the mentioned	[ ]
84	Both the CISC and RISC architectures have been developed to reduce the _____ a)Cost b) Time delay c) Semantic gap d) All of the mentioned	[ ]
85	Which control refers to the track of the address of instructions a)Data control b) Register control c) Program control d)None of these	[ ]
86	In program control the instruction is set for the statement in: a)Parallel b)Sequence c)Both a &b d) None	[ ]
87	SIMD stands for: a)System instruction multiple data b) Scale instruction multiple data c)Symmetric instruction multiple data d) Single instruction multiple data	[ ]
88	MIMD stands for: a)Multiple input multiple data b) Memory input multiple data c)Multiple instruction multiple data d) Memory instruction multiple data	[ ]
89	Which is a method of decomposing a sequential process into sub operations? a)Pipeline b)CISC c) RISC d)Database	[ ]
90	Which are the types of array processor? a)Attached array processor b) SIMD array processor c)Both d)None	[ ]

91	Which type of register holds a single vector containing at least two read ports and one write ports a)Data system b)Database c)Memory d)Vector register	[ ]
92	Which is used to speed-up the processing: a)Pipeline b) Vector processing c) Both d) None	[ ]
93	Which processor is a peripheral device attached to a computer so that the performance of a computer can be improved for numerical computations? a)Attached array processor b) SIMD array processor c) Both d) None	[ ]
94	Which processor has a single instruction multiple data stream organization that manipulates the common instruction by means of multiple functional units? a)Attached array processor b)SIMD array processor c)Both d)None	[ ]
95	Processor without structural hazard is a)Faster b)Slower c)Have longer clock cycle d) Have larger clock rate	[ ]
96	Simplest scheme to handle branches is to a)Flush pipeline b)Freezing pipeline c)Both a and b d)Depth of pipeline	[ ]
97	Splitting cache into separate instructions and data caches or by using a set of buffers, usually called a)Cache buffer b)Data buffer c) Instruction buffer d)None of above	[ ]
98	With separate adder and a branch decision made during ID, there is only a a)1-clock-cycle stall on branches b) 2-clock-cycles stall on branches c) 3-clock-cycles stall on branches d) 4-clock-cycles stall on branches	[ ]
99	Load instruction has a delay or latency that cannot be eliminated by forwarding, other technique used is a)Pipeline interlockb)Deadlock c)Stall interlock d) Stall deadlock	[ ]
100	If event occurs at same place every time program is executed with same data and memory allocation, then event is known as a)Stalled b) Synchronous c) Delayed d) Asynchronous	[ ]
	Pipeline overhead arises from combination of pipeline register delay and a)Hit rate b) Clock cycle c)Cycle rate d)Clock skew	[ ]
	Each of clock cycles from previous section of execution, becomes a a)Pipe stage b) Previous stage c) Stall d) Processor cycle	[ ]
101	Exceptions that occur within instructions are usually a)Synchronous b)Asynchronous c) Pipelined d)Blocked	[ ]
102	When compiler attempts to schedule instructions to avoid hazard; this approach is called a)Compiler b)Static scheduling c) Dynamic scheduling d) Both a and b	[ ]
103	Pipelining increases CPU instruction a) Size b) Through put c) Cycle rate d) Time	[ ]
104	Sum of contents of base register and sign-extended offset is used as a memory address, sum is known as a) ALU instructions b) Through put c) Effective address d) Load and store instructions	[ ]
105	Process of letting an instruction move from instruction decode stage into execution stage of this pipeline is usually called a) Canceling b) Instruction issue c) Nullifying d) Branch prediction	[ ]
106	If an exception is raised and the succeeding instructions are executed completely, then the processor is said to have _____ a) Exception handling b) Imprecise exceptions c) Error correction d) None	[ ]
107	The product of 1101 & 1011 is _____ a) 10001111 b) 10101010 c) 11110000 d) 11001100	[ ]
108	Code containing redundant loads, stores, and other operations that might be eliminated by an optimizer, is a) Optimized clock b) Unoptimized clock c) Optimized code d) Unoptimized code	[ ]
109	Delays arising from use of a load result 1 or 2 cycles after loads, refers as a) Data stall b) Control stall c) Branch stall d) Load stall	[ ]
110	Situations that prevent next instruction in instruction stream, from executing during its designated clock cycle are known a) Pipe stage b) Previous stage c) Hazards d) Processor cycle	[ ]
111	The product of -13 & 11 is a) 1100110011 b) 1101110001 c) 1010101010 d) 1111111000	[ ]

112	The method used to reduce the maximum number of summands by half is _____ a) Fast multiplication b) Bit-pair recording c) Quick multiplication d) None	[ ]
113	The digital information is stored on the hard disk by _____ a) Applying a suitable electric pulse b) Applying a suitable magnetic field c) Applying a suitable nuclear field d) By using optic waves	[ ]
114	A hard disk with 20 surfaces will have _____ heads. a) 10 b) 5 c) 1 d) 20	[ ]
115	The read and write operations usually start at _____ of the sector. a) Center b) Middle c) From the last used point d) Boundaries	[ ]
116	The associatively mapped virtual memory makes use of _____ a) TLB b) Page table c) Frame table d) None of the mentioned	[ ]
117	If the instruction Add R1, R2, R3 is executed in a system which is pipelined, then the value of S is (Where S is a term of the Basic performance equation) a)3 b) ~2 c) ~1 d) 6	[ ]
118	Two processors A and B have clock frequencies of 700 Mhz and 900 Mhz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster? a)A b) B c) Both take the same time d) Insufficient information	[ ]
119	An effective to introduce parallelism in memory access is by _____ a)Memory interleaving b) TLB c) Pages d) Frames	[ ]
120	The performance depends on _____ a)The speed of execution only b) The speed of fetch and execution c) The speed of fetch only d) The hardware of the system only	[ ]
121	A common measure of performance is _____ a)Price/performance ratio b) Performance/price ratio c) Operation/price ratio d) None	[ ]
122	The bits 1 & 1 are recorded as _____ in bit-pair recording. a)-1 b) 0 c) +1 d) Both -1 and 0	[ ]
123	The fastest data access is provided using _____. a) Caches b) DRAM's c) SRAM's d) Registers	[ ]
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